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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,213	02/27/2004	Chiung-Pin Wang	BHT-3167-179	4703

7590 06/07/2005

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EXAMINER	
CHEN, WEN YING PATTY	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,213	WANG, CHIUNG-PIN	
	Examiner	Art Unit	
	Wen-Ying P. Chen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 2 is objected to because of the following informalities: Claim 2 refers to said gate electrodes, which has no previous reference in either claim 2 or the depending claim of claim 1. For examining purposes, the "said gate electrodes" will be treated as "gate electrodes". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8 and 10-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Jung et al. (US 2004/0051836A1).

With respect to claim 1: Jung et al. disclose in Figure 5 a flat panel display comprising: a glass substrate (element 110), which is divided into a displaying area (element D) and a surrounding frame area (element S_2), wherein the displaying area further comprising a plurality of pixel devices, each pixel device comprising a thin film transistor (TFT) (element 120) utilized as a switch; a plurality of first conductive lines (element CL_1), a dielectric layer (element 127)

covering the first conductive lines; and a plurality of second conductive lines (element CL_2) formed on top of the dielectric layer.

As to claims 2 and 4: Jung et al. disclose that the first conductive lines and the gate electrodes of the TFTs are formed in a metal layer and the first conductive lines are formed such that they are positioned along a boundary of the displaying area with a predetermined interval (Paragraphs 0065 and 0066).

As to claims 3 and 5: Jung et al. disclose that the second conductive lines and the source/drain electrodes of the TFTs are formed in a metal layer and the second conductive lines are formed such that they are positioned along a boundary of the displaying area with a predetermined interval (Paragraphs 0074, 0075 and 0078).

As to claim 6: Jung et al. disclose that the dielectric layer is formed of silicon nitride (Paragraph 0067).

As to claims 7 and 8: Jung et al. disclose in Figures 6A-6F the method of forming a flat panel comprising the steps of: forming a plurality of gate lines (element GL) and a plurality of first conductive lines (element CL_1) on a glass substrate (element 110) by first forming a metal layer (element 111) and then by etching of the metal layer, wherein the first conductive lines are connected to the gate lines; forming a dielectric layer (elements 122 and 127) to cover the gate lines and the first conductive lines; and forming a plurality of sources (element 125), drains (element 126), and second conductive lines (element CL_2) on the dielectric layer, and having the second conductive lines connect to rest of the gate lines.

As to claims 10-12: Jung et al. further disclose in Figure 6F that the method comprises steps of forming the gate lines (element GL) in a displaying area (element D) and the first and

second conductive lines (elements CL_1 and CL_2) in a surrounding frame area (element S_2), wherein the first and second conductive lines are positioned with a predetermined interval.

As to claim 13: Jung et al. disclose in Paragraph 0067 that the dielectric layer is formed of silicon nitride.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al. (US 2004/0051836A1) in view of Takahashi et al. (US 2003/0112382A1).

Jung et al. disclose in Figures 6A-6G the fabrication method as stated in claim 7, and further comprising the steps of forming a second metal layer (element 114) over the dielectric layer (element 122); etching the second metal layer to form sources (element 125), drains

(element 126), and second conductive lines (element CL_2); forming a passivation layer (element 130, as shown in Figure 5) to cover the source, drain, and the second conductive lines.

Jung et al. lack to specifically disclose that openings exposing the rest of gate lines and the second conductive lines are formed through etching and that a plurality of connecting structures are formed on top of the passivation layer as to connect the second conductive lines with the rest of the gate lines.

However, Takahashi et al. teach in Paragraphs 0161-0177 and Figures 6A and 6B the steps of forming a passivation layer (element PSV), exposing the gate lines and conductive lines by etching, and forming of a plurality of connecting structures (element ITO) so that the conductive lines are connected to the gate lines.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the second conductive lines to the gate lines as taught by Takahashi et al. when fabricating the display panel as taught by Jung et al. since Takahashi et al. teach that a reliable connection between the gate lines and the conductive lines can thus be obtained (Paragraph 0166).

Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung et al. (US 2004/0051836A1) in view of Hinata (US 2001/0022644).

Jung et al. disclose in Figure 1 a liquid crystal display comprising a color filter layer (element 200), a liquid crystal layer (element 300), a TFT panel (element 100), and in Figure 2 a driving circuit (element 150) having connection with the gates of the TFTs through conductive lines. Jung et al. further disclose in Figures 5, and 6A-6G that the TFT panel further comprising:

a rectangular glass substrate (element 110) divided into a displaying area (element D) and a surrounding frame area (element S_2), a plurality of pixel devices each device comprising a thin film transistor (TFT) (element 120) utilized as a switch; a plurality of first conductive lines (element CL_1) formed in the frame area positioned with a predetermined interval, wherein the first conductive lines and the gate electrodes are formed in a metal layer (element 111); a dielectric layer (element127) formed of silicon nitride (Paragraph 0067) deposited on top of the first conductive lines at the frame area; and a plurality of second conductive lines (element CL_2) formed on top of the dielectric layer and positioned with a predetermined interval having connection to the rest of the gate lines, wherein the second conductive lines and the source and drain electrodes are formed in a metal layer (element 114).

Jung et al. fail to specifically disclose a backlight module.

However, Hinata discloses in Figure 2 a liquid crystal display, which comprises of a back light module (element 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a backlight module as taught by Hinata with the liquid crystal display as taught by Jung et al. so that illumination of the display can be provided with the light source.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ishige et al. (US 2004/0012744) as an alternative display device, wherein the

conductive lines connecting to the gate lines are stacked so as to provide a narrower peripheral area of the display device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wen-Ying P. Chen whose telephone number is (571)272-8444. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wen-Ying P Chen
Examiner
Art Unit 2871

wpc

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SUPERVISORY PATENT EXAMINER
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